

REMARKS

This is in response to the Office Action dated March 24, 2005. Claim 4 has been canceled, and its subject matter added to claim 1. New claim 24 has been added. Thus, claims 1-3 and 5-24 are now pending.

The title has been amended as suggested by the Examiner.

It is noted that the species of Figs. 8-9 was elected in the response filed January 24, 2005.

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Taki. This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 1 as amended requires that "a predetermined scheme is used to connect between the first cell and the second cell, between the plurality of transistors in the first cell, and between the PMOS transistor section and the NMOS transistor section in the second cell, and wherein the first cell functions as a logic operation circuit for outputting data, and the second cell functions as at least one of a driver circuit for driving the logic operation circuit or a data retaining circuit for retaining data output by the logic operation circuit." The cited art fails to disclose or suggest these features of claim 1. For example, Taki fails to disclose or suggest a second cell being able to function as a data retaining circuit for retaining data output by the logic operation circuit.

Taki discloses a logic gate cell featuring a small area and low power consumption which is constructed of a circuit of two inverting logic gates connected in series in a layout of four-step diffusion regions (e.g., see Abstract of Taki). In particular, the inverting logic gates refer to a NAND gate, a NOR gate, a NOT gate, and an AND-NOR compound gate and an OR-NAND compound gate (col. 1, lines 16-18). Taki discloses the circuit arrangement for the connection of the two inverting logic gates by employing two PMOS transistor diffusion regions and two NMOS transistor diffusion regions, where the first inverting logic gate is realized by the two

internal diffusion regions and the second inverting logic gate is realized by the two external diffusion regions (e.g., col. 2, lines 21-43). An output of the first inverting logic gate is connected to one of inputs of the second inverting logic gate. A particular scheme is used to connect between the first inverting logic gate and second inverting logic gate.

In Figs. 49A and 49B, Taki discloses an AND-OR circuit with the circuit diagram shown in Fig. 50. The circuit diagram comprises a first inverting logic gate 1, which is connected to a second inverting logic gate 2. As shown in the circuit diagram, the first inverting logic gate 1 comprises a PMOS transistor section and an NMOS transistor section. Furthermore, the PMOS transistor second includes a first PMOS transistor and a second PMOS transistor connected in series. Similarly, the NMOS transistor section includes a first NMOS transistor and a second NMOS transistor connected in series. The connection scheme is shown in Figs. 47A, 47B, 48A and 48B.

Amended claim 1 requires that the “second cell functions as at least one of a driver circuit for driving the logic operation circuit or a data retaining circuit for retaining data output by the logic operation circuit.” An example advantage of the second cell functioning as a data retaining circuit is that only an active circuit block is in the operating state while an inactive circuit block is in the standby state. Thus, a standby current involved in a leakage current in this example situation can be reduced, whereby power is not wasted and a low power consumption semiconductor IC can be achieved (e.g., pg. 29, lines 12-22). Taki fails to disclose or suggest a second cell being able to function as a data retaining circuit for retaining data output by the logic operation circuit.

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Moreover, for example, the first and second cells called for in claim 1 make possible the example advantage of providing a semiconductor IC in which the plurality of types of logic functions can be realized using a small number of types of cells.

Claim 24 requires that "the second cell functions as a data retaining circuit for retaining data output by the logic operation circuit." Taki fails to disclose or suggest this requirement of claim 24.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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